



US007079972B1

(12) **United States Patent**
Wood et al.

(10) **Patent No.:** **US 7,079,972 B1**
(45) **Date of Patent:** **Jul. 18, 2006**

(54) **APPARATUS AND METHOD FOR
TEMPERATURE CONTROL OF
INTEGRATED CIRCUITS**

(75) Inventors: **Peter R. Wood**, Los Altos, CA (US);
Narc V. Peralta, Union City, CA (US);
Frank S. Madren, Los Gatos, CA
(US); **Dileep Sivasankaran**, Fremont,
CA (US)

(73) Assignee: **GarrettCom, Inc**, Fremont, CA (US)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 111 days.

(21) Appl. No.: **10/649,371**

(22) Filed: **Aug. 27, 2003**

Related U.S. Application Data

(60) Provisional application No. 60/418,897, filed on Oct.
15, 2002.

(51) **Int. Cl.**
G01R 27/28 (2006.01)
G01R 21/02 (2006.01)

(52) **U.S. Cl.** **702/117; 324/760**

(58) **Field of Classification Search** **702/117,**
702/120, 130; 219/208, 209, 497, 501, 505,
219/388, 494, 481; 324/755-760, 765, 537;
165/80.2, 80.3, 80.4; 374/102; 347/17,
347/18, 56, 60

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,860,166 A * 8/1989 Nicholls 361/792
5,638,097 A * 6/1997 Takayanagi et al. 347/7
5,844,208 A * 12/1998 Tustaniwskyj et al. 219/494
5,889,462 A * 3/1999 Rana et al. 338/254
6,476,508 B1 11/2002 Strnad
6,510,400 B1 1/2003 Moriyama
2005/0122689 A1 6/2005 Pozzuoli
2006/0007614 A1 1/2006 Pozzuoli et al.

OTHER PUBLICATIONS

LM56 Dual Output Low Power Thermostat, pp. 1-12; 2001
National Semiconductor Corporation.

* cited by examiner

Primary Examiner—Bryan Bui

Assistant Examiner—Meagan S Walling

(74) *Attorney, Agent, or Firm*—Okamoto & Benedicto LLP

(57) **ABSTRACT**

One embodiment disclosed relates to an apparatus for tem-
perature control of an integrated circuit on a circuit board.
The apparatus includes a first resistor on the circuit board, a
second resistor on the circuit board, and a heat conductive
material. The heat conductive material is attached to both the
first and second resistors and to a surface of a package
containing the integrated circuit. Another embodiment dis-
closed relates to an apparatus that provides both cooling and
heating functionality in order to maintain the operational
temperature of the IC within an acceptable range.

20 Claims, 4 Drawing Sheets